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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,466	SATHE, AJIT V.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this c mmunication appears on th c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *appeals brief filed on August 19, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *14-39 and 46-64* is/are pending in the application.

4a) Of the above claim(s) *19,24-26,32,37-39,50,57 and 62-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-18,20-23,27-31,33-36,46-49,51-56 and 58-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Revi w (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Dat _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Pursuant to further review after receipt of the appeals brief filed on August 19, 2003, examiner has discovered that, while the arguments are not persuasive, there is a great deal of confusion about the "thin core" and "coreless" substrate as claimed. Therefore, PROSECUTION IS HEREBY REOPENED. Detailing a new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description

requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

"Thin core" or "coreless" substrate is explained in the disclosure by a working example. However, "core" as defined in The IEEE Standard Dictionary of Electronic and Electronics Terms, Sixth Edition, is the central layer or basic support of certain types of laminated media. For a person of ordinary skill in the art, a core layer in the substrate will be any layer on which other layers are formed. The core layer may be located in the center of the substrate or at any other location in the substrate.

In the specification there is no explanation of what is a "core". There is only example of layer, which meets the definition above. The example identifies the thickness for the core layer as 0.1 to .5 mm, and more specifically about 0.4 mm. However, it is not clear, whether, all the layers are having the thickness as described, less than 0.5 mm, or there may be a presence of a layer with a thickness more than 0.5 mm. Also, if all the layers are with the thickness of 0.5 mm or less, why couldn't any of the layers be a core layer, and that makes the concept of the coreless substrate unclear. It is unclear for a person of ordinary skill in the art to understand what constitute a thin core or coreless substrate according to the specification and what is the difference between the coreless and thincore substrate.

Claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. "Thin core" or "coreless" substrate is explained in the disclosure by a working example. However, "core" as defined in The IEEE Standard Dictionary of Electronic and Electronics Terms, Sixth Edition, is the central layer or basic support of certain types of laminated media. For a person of ordinary skill in the art, a core layer in the substrate will be any layer on which other layers are formed. The core layer may be located in the center of the substrate or at any other location in the substrate.

In the specification there is no explanation of what is a "core". There is only example of layer, which meets the definition above. The example identifies the thickness for the core layer as 0.1 to .5 mm, and more specifically about 0.4 mm. However, it is not clear, whether, all the layers are having the thickness as described, less than 0.5 mm, or there may be a presence of a layer with a thickness more than 0.5 mm. Also, if all the layers are with the thickness of 0.5 mm or less, why couldn't any of the layers be a core layer, and that makes the concept of the coreless substrate unclear. It is unclear for a person of ordinary skill in the art to understand what constitute a thin core or coreless substrate according to the specification and what is the difference between the coreless and thincore substrate.

Therefore, for the examination purpose, the examiner assumes the coreless / thin core substrate is a substrate with each of the layers constituting the substrate having a thickness not more than 0.5 mm, excluding the stiffener.

Further, regarding claims 52-56 and 58-61, the applicant is claiming an electronic system comprising at least one input/output device. However, the input / output device is not described in the disclosure.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 14-18, 20-23, 27-31, 33-36, 46-49, 51-56 and 58-61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In all of the above claims the applicant is claiming a stiffener to provide stiffening to one of a "thin core and coreless substrate". It is not clear to the examiner as to what is meant by a "thin core and coreless substrate".

"Thin core" or "coreless" substrate is explained in the disclosure by a working example. However, "core" as defined in The IEEE Standard Dictionary of Electronic and Electronics Terms, Sixth Edition, is the central layer or basic support of certain types of laminated media. For a person of ordinary skill in the art, a core layer in the substrate

will be any layer on which other layers are formed. The core layer may be located in the center of the substrate or at any other location in the substrate.

In the specification there is no explanation of what is a "core". There is only example of layer, which meets the definition above. The example identifies the thickness for the core layer as 0.1 to .5 mm, and more specifically about 0.4 mm. However, it is not clear, whether, all the layers are having the thickness as described, less than 0.5 mm, or there may be a presence of a layer with a thickness more than 0.5 mm. Also, if all the layers are with the thickness of 0.5 mm or less, why couldn't any of the layers be a core layer, and that makes the concept of the coreless substrate unclear. It is unclear for a person of ordinary skill in the art to understand what constitute a thin core or coreless substrate according to the specification and what is the difference between the coreless and thincore substrate.

Therefore, for the examination purpose, the examiner assumes the coreless / thin core substrate is a substrate with each of the layers constituting the substrate having a thickness not more than 0.5 mm, excluding the stiffener.

6. Claims 23, 36 and 61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 23, 36 and 61, "if a main body of the stiffener is electrically conductive, the stiffener further includes an insulator to electrically insulate electrical members on stiffener opposing areas of the substrate" is indefinite. The existence of the conductive

stiffener including the insulator in the final product is unclear, because of the "if" statement. This makes the scope indefinite.

Furthermore, it is unclear whether applicant is claiming that the stiffener is conductive or not.

To apply a prior art, the stiffener was considered conductive.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 14-18, 20-23, 27-31, 33-36, 46-49 and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsukamoto, US Patent No. 5,841,194.

Regarding claim 14, Tsukamoto discloses thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate (element 108, figure 1-4, because they show a thin substrate of about 0.1mm, column 7, line 39-42), and

a stiffener (element 106, figure 1) to provide stiffening support to the one of a thin-core and coreless substrate (column 4, line 59-67).

Regarding claim 27, Tsukamoto discloses a packaged integrated circuit (1C) comprising:

an IC (element 201, figure 4, 5 and 6), and

a thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate (element 108, figure 1-4, because they show a thin substrate of about 0.1mm, column 7, line 39-42), and a stiffener (element 106, figure 1) to provide stiffening support to the one of a thin-core and coreless substrate (column 4, line 59-67 and thin substrate of 0.1 mm used for the carrier substrate 108, column 7, line 39-42).

Regarding claim 46, Tsukamoto discloses a thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate (element 108, figure 1-4, because they show a thin substrate of about 0.1mm, line 39-42), and

a stiffener (element 106, figure 1) secured onto the at least one of a thin-core and coreless substrate of the integrated circuit printed circuit board (IC-PCB) carrier package to provide stiffening support thereto (column 4, line 59-67 and thin substrate of 0.1 mm used for the carrier substrate 108, column 7, line 39-42).

Regarding claims15, 28 and 47, Tsukamoto further discloses flip chip ball grid array carrier package (see figure 4, column 7, line 10-29).

Regarding claims16, 29 and 48, Tsukamoto further discloses the stiffener member (element 106, figure 1) made of glass (glass epoxy material, column 5, line 17-20).

Regarding claims 17, 30 and 49, Tsukamoto further discloses the stiffener (element 106) being planar and mounted to a die-side major planar surface of the substrate (see figure 4).

Regarding claims18 and 31, Tsukamoto further discloses an internal window in the stiffener (see figure 1, 2 and 4).

Regarding claims 20 and 33, Tsukamoto further discloses the stiffener having an above substrate-plane height less than an above substrate-plane height, when mounted, of an IC die (see figure 4, column 7, line 39-44).

Regarding claims 21 and 34, Tsukamoto further discloses top surface of the stiffener co-planar with the top surface of the semiconductor chip when mounted (see figure 5 and 6).

Regarding claims 22, 35 and 51, Tsukamoto further discloses, the stiffener can co-support a heat sink (see figure 10)

R garding claims 23 and 36, Tsukamoto further discloses stiffener made of copper or aluminum, which are electrically conductive and further include an insulator to electrically insulate electrical members on the stiffener opposing areas of the substrate (figure 6, column 8, line 1-10).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 14, 27 and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Ho, US Patent No. 6,287,890.

Regarding claim 14, Ho discloses thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate (element 12, figure 1, because it shows thin film interconnect metal layers 18 and 20, and thin film of epoxy layer, column 6, line 30-60 and column 7, line 35 to column 8, line 7),

a stiffener (element 14, figure 1) to provide stiffening support to the one of a thin-core and coreless substrate (column 6, line 30-60 and column 7, line 35 to column 8, line 7).

Regarding claim 27, Ho discloses a packaged integrated circuit (1C) comprising:

an IC (element 16), and

a thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate (element 12, figure 1, because it shows thin film interconnect metal layers 18 and 20 and thin film of epoxy layer, column 6, line 30-60 and column 7, line 35 to column 8, line 7), and a stiffener (element 14, figure 1) to provide stiffening support to the one of a thin-core and coreless substrate (column 6, line 30-60 and column 7, line 35 to column 8, line 7).

Regarding claim 46, Ho discloses a thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate (element 12, figure 1, because it shows thin film interconnect metal layers 18 and 20 and thin film of epoxy layer, column 6, line 30-60 and column 7, line 35 to column 8, line 7), and

a stiffener (element 14, figure 1) secured onto the at least one of a thin-core and coreless substrate of the integrated circuit printed circuit board (IC-PCB) carrier

package to provide stiffening support thereto (column 6, line 30-60 and column 7, line 35 to column 8, line 7).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 52-56 and 58-61 rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto, as applied to claims 14-18, 20-23, 27-32, 33-36, 46-49 and 51 above, and further in view of Smith et al., US Patent No. 5,694,297 and Werther, US Patent No. 5,515,241.

Regarding claim 52, the applicant is claiming an electronic system comprising packaged integrated circuit (IC) having an IC, and a thin-core or coreless integrated circuit printed circuit board (IC-PCB) carrier package having one of a thin-core and coreless substrate, and a stiffener to provide stiffening support to the one of a thin-core and coreless substrate; a receiving socket to receive the packaged IC.

Tsukamoto discloses all the element of the claim, except a receiving socket to receive the packaged IC.

However, the field of invention of Tsukamoto is to have a semiconductor device having a carrier substrate equipped with the semiconductor chip (column 1, line 5-10). Tsukamoto discloses the packaged IC with pads on the other side of the substrate for connecting the package to other device (figure 1, 3-6).

Werther discloses prepackaged packages with pins mounted on the socket in the circuit board, which will reduce the difficulty and cost of installation and testing, see figure 4-5.

Smith et al., discloses an integrated circuit mounting structure with IC package 102 with pins with respective socket in the board.

As disclosed by Werther and Smith, it is well known in the art to have an IC package with pins to be connected in a respective socket in the electronic system.

A person of ordinary skill in the art would have been motivated to use pins on the other side of the substrate in the semiconductor device of Tsukamoto, to reduce difficulty and cost of installation and testing.

Therefore, it would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the IC package of Tsukamoto in the electronic device with a socket in the device to receive the IC package, from the teachings of Smith et al., and Werther, in order to reduce cost of installation and testing, thereby meeting the limitation of electronic system comprising a receiving socket to receive the packaged IC.

R garding claim 53, the modified structure of Tsukamoto further discloses flip chip ball grid array carrier package (see figure 4, column 7, line 10-29).

Regarding claim 54, the modified structure of Tsukamoto further discloses the stiffener member (element 106, figure 1) made of glass (glass epoxy material, column 5, line 17-20).

Regarding claims 55, the modified structure of Tsukamoto further discloses the stiffener (element 106) being planar and mounted to a die-side major planar surface of the substrate (see figure 4).

Regarding claim 56, the modified structure of Tsukamoto further discloses an internal window in the stiffener (see figure 1, 2 and 4).

Regarding claim 58, the modified structure of Tsukamoto further discloses the stiffener having an above substrate-plane height less than an above substrate-plane height, when mounted, of an IC die (see figure 4, column 7, line 39-44).

Regarding claim 59, the modified structure of Tsukamoto further discloses top surface of the stiffener co-planar with the top surface of the semiconductor chip when mounted (see figure 5 and 6).

Regarding claim 60, the modified structure of Tsukamoto further discloses, the stiffener can co-support a heat sink (see figure 10)

Regarding claim 61, the modified structure of Tsukamoto further discloses stiffener made of copper or aluminum, which are electrically conductive and further include an insulator to electrically insulate electrical members on the stiffener opposing areas of the substrate (figure 6, column 8, line 1-10).

13. Claims 14-18, 20-23, 27-31, 33-36, 46-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al., US Patent No. 6,020,221, in view of Yamashita et al., US Patent No. 5,777,387 and Murasawa, US Patent 5,841,188.

Regarding claim 14, Lim discloses an integrated circuit printed circuit board (IC-PCB) carrier package having substrate (element 14, figure 2-8), and

a stiffener (element 20, figure 2-8) to provide stiffening support to the substrate (column 4, line 40-50).

Lim fail to disclose the substrate is thin core or coreless substrate. However, Lim discloses that substrate can be made of other known substrate material such as PTFE (Teflon), polyamide tape, BT-FR4 and BT-FR5, column 5, line 55-60, and in a thin film single layer construction, column 5, line 64-67.

Yamashita et al., in the background disclosure discloses that polyimide is generally used as the base material with a tape thickness of about 50-125 μm, in a BGA package film carrier with a stiffener to avoid warping and waviness, column 2, line 39-46.

Murasawa discloses a tape carrier with a preferable thickness of polyimide tape 3 less than or equal to 50 μm.

As disclosed by Yamashita and Murasawa, it is well known in the art to use a tape with thickness of 50-125 μm or less than 50 μm for a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device.

Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide the package of Lim with a thin tape having a thickness of less than 150 μm in order to have a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device.

Regarding claim 27, Lim discloses a packaged integrated circuit (1C) comprising:

an IC (element 12, figure 2-8), and

an integrated circuit printed circuit board (IC-PCB) carrier package having a substrate (element 14, figure 2-8), and a stiffener (element 20, figure 2-8) to provide stiffening support to the substrate (column 4, line 40-50).

Lim fail to disclose the substrate is thin core or coreless substrate. However, Lin discloses that substrate can be made of other known substrate material such as PTFE (Teflon), polyamide tape, BT-FR4 and BT-FR5, column 5, line 55-60, and in a thin film single layer construction, column 5, line 55-60, and in a thin film single layer construction, column 5, line 64-67.

Yamashita et al., in the background disclosure discloses that polyimide is generally used as the base material with a tape thickness of about 50-125 μm, in a BGA package film carrier with a stiffener to avoid warping and waviness, column 2, line 39-46.

Murasawa discloses a tape carrier with a preferable thickness of polyimide tape 3 less than or equal to 50 μm.

As disclosed by Yamashita and Murasawa, it is well known in the art to use a tape with thickness of 50-125 μm or less than 50 μm in order to have a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device.

Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide the package of Lim with a thin tape having a thickness of less than 150 μm in order to have a cost effective IC package.

Regarding claim 46, Lim discloses an integrated circuit printed circuit board (IC-PCB) carrier package having a substrate (element 14, figure 2-8), and

a stiffener (element 20, figure 2-8) secured onto the substrate of the integrated circuit printed circuit board (IC-PCB) carrier package to provide stiffening support thereto (column 4, line 40-50).

Lim fail to disclose the substrate is thin core or coreless substrate. However, Lin discloses that substrate can be made of other known substrate material such as PTFE (Teflon), polyamide tape, BT-FR4 and BT-FR5, column 5, line 55-60, and in a thin film single layer construction, column 5, line 55-60, and in a thin film single layer construction, column 5, line 64-67.

Yamashita et al., in the background disclosure discloses that polyimide is generally used as the base material with a tape thickness of about 50-125 μm, in a BGA package film carrier with a stiffener to avoid warping and waviness, column 2, line 39-46.

Murasawa discloses a tape carrier with a preferable thickness of polyimide tape 3 less than or equal to 50 μm.

As disclosed by Yamashita and Murasawa, it is well known in the art to use a tape with thickness of 50-125 μm or less than 50 μm for a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device.

Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide the package of Lim with a thin tape having a thickness of less than 150 μm in order to have a semiconductor package which can be interconnectably mounted on underlying semiconductor package substrate for a high density semiconductor device.

Regarding claims15, 28 and 47, the modified assembly of Lim further discloses flip chip ball grid array carrier package (see figure 8, column 3, line 57-60).

Regarding claims16, 29 and 48, the modified assembly of Lim further discloses the stiffener member stamped form a metallic material (column 5, line 18-24).

Regarding claims 17, 30 and 49, the modified assembly of Lim further discloses the stiffener being planar for mounting to a die-side major planar surface of the substrate (see figure 8).

Regarding claims18 and 31, the modified assembly of Lim further discloses an internal window in the stiffener (see figure 8).

Regarding claims 20 and 33, the modified assembly of Lim further discloses the above substrate height of the stiffener equal to that of the above substrate height of the semiconductor chip (see figure 8).

Regarding claims 21 and 34, the modified assembly of Lim further discloses top surface of the stiffener co-planar with the top surface of the semiconductor chip (see figure 8).

Regarding claim 22, 35 and 51, the modified assembly of Lim further discloses, the stiffener can co-support a heat sink as shown in figure 8, a protective layer 44 fabricated of a metal such as copper.

Regarding claims 23 and 36, the modified assembly of Lim further discloses stiffener made of copper, which is conductive with an epoxy resin layer in-between (column 4, line 40-50, see figure 8).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Suminoe et al., discloses a tape ball grid array semiconductor with a radiating plate 7 made of metal function as a reinforcing member, column 11, lien 60-65.

Plepys et al., discloses package integrated circuit comprising a flexible circuit with a stiffener.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

I B Patel
Examiner
GAU: 2827

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800